ABSTRACT

Output buffer slew rate variation over variations in load capacitance is minimized by dividing output voltage transitions into distinct time and output current segments. During the first time segment, the first drive stage with the smallest current is employed. After subsequent delays, additional drive stages are employed and the load current is sequentially increased. Each drive stage employs a specifically sized feedback device which, depending upon its dimensions will provide either parasitic capacitance to slow transitions or positive feedback to speed up transitions. The first stages are sized to incorporate parasitic capacitance, resulting in little change in the settling time of small capacitance loads over prior art output buffers. Latter stages use positive feedback to quicken the transition time which dramatically improves the settling time for larger load capacitances over prior art output buffers.